REMARKS

Claims 1-6, 8-17, and 24-26 are pending in this application. Claims 18-21 are withdrawn and claim 7, 22, and 23 are canceled herein. Claims 1, 2, 3, 11, and 13 have been amended and claims 24-26 have been added herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

On page 3 of the Office Action, the Examiner rejected claims 1-3 and 5-10 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,339,239 to Alsmeier, *et al.* However, although claims 12-15 were not mention on page 3 of the Office Action, these claims were discussed in page 5. It is believed the Examiner also intended to reject claims 12-15 under 35 U.S.C. 102(b) and, therefore, these claims have been treated as being rejected under 35 U.S.C. 102(b). Dependent claim 7 has been canceled and its limitations have been added to independent claim 1.

The single original claim 1 has been amended so that it now clearly patentably defines over the Alsmeier, *et al.* patent and all other references of record. More specifically, claim 1 has been amended to now require the channel region of the access transistor to be formed in the trench as was originally required by the canceled claim 7. In addition, it is noted that the original claim 1 required that the word line be formed within the semiconductor substrate. The Examiner alleges on page 4 of the rejection that FIGs. 4 and 6 of Alsmeier, *et al.* show the channel region being formed in the trench. This is simply not correct. In FIG. 4, the channel regions 53 and 55 are part of the active region and certainly are not in the DT's (deep trenches) illustrated in FIG. 4. Similarly, the channel region of the transistors shown in FIG. 6 is in the P-well of the substrate between the diffusion regions 101 and 105 along side the gate oxide 104. These channels simply

are not in the deep trenches (DT's). Further, Alsmeier, *et al.* did not disclose, much less teach, the original limitation in claim 1 that the word line is formed within the semiconductor substrate. Therefore, it is respectfully submitted that the original claim 1 was not anticipated by Alsmeier, *et al.* More specifically, since claim 1 now requires still a further limitation not disclosed by Alsmeier, *et al.*, it is submitted that claim 1 does now clearly patentably define over and is not anticipated by Alsmeier, *et al.*

Dependent claims 2, 3, 12, and 15 include some minor clarifying amendments, however, no new subject matter has been added. Therefore, claims 2-15 are now allowable for their own limitations as well as for depending from a claim deemed allowable. New claims 24 and 25 depend from amended claims 1 and 6 and are also allowable for their own limitations as well as for depending from a claim deemed allowable.

New independent claim 26 is allowable for all of the reasons discussed with respect to claim 1 but also includes the further limitations of original claim 10.

Further, Alsmeier, *et al.* relates to a layout pattern for increasing the spacing between the deep trenches of one cell pair and the deep trenches of an adjacent cell pair in an array of semiconductor DRAM cell pairs. Each of the DRAM cell pairs share a common contact to bitlines arranged in one direction and each cell of each cell pair is coupled to a gate conductor arranged orthogonal to the bitlines. The layout pattern is formed by positioning the deep trenches of all of the DRAM cell pairs along alternate bitlines so they are offset from the bitlines along gate conductors in opposing directions. The deep trenches of all of the remaining bitlines are also offset from the bitlines in opposing directions opposite to the opposing directions of the trenches along the alternate bitlines so as to form a herringbone pattern of cells as shown in FIG. 5 of Alsmeier, *et al.*

FIG. 4 of Alsmeier, *et al.* depicts a cross-section view through planar transistor cell pairs, *and the active wordlines 41 and 43 pass over the active area, and the passing wordlines 45 and 47 pass over the DT regions 49 and 51.* Field effect transistors (FETs) are formed by the active wordlines 41 and 43 where they pass over the active area to form the channel regions 53 and 55. The passing wordlines serve as active wordlines in directly adjacent DT cells.

As can be seen in FIG. 6, wordlines 110 and 111 are separated by bitline contact 112, which connects the source diffusion region to bitline 113 (Note: the diffusion region is identified as 105 in the FIG. 6, but as 102 in the specification). The wedge-shaped regions between wordlines 110-111 and bitline contact 112, and the rectangular regions on top of wordlines 110 and 111 are insulating regions that insulate the wordlines and gate conductors from bitline contact 112. *Thus, as shown in FIG. 6, the adjacent wordlines 110 and 111 pass over the active semiconductor area of the DRAM cell array. They are not formed in the semiconductor substrate.*

As discussed above, the amended claim 1 and the newly presented claim 26 of the present invention are novel with respect to Alsmeier, *et al.* for the following reasons:

- the channel region of the access transistor is formed in the trench of the memory cell, and

- the control electrode regions of neighboring access transistors are connected by a word line formed in the semiconductor substrate.

In addition, as discussed below, these features are not rendered obvious under 35 U.S.C. 103(a) by Alsmeier, *et al.*

As is known, efforts for developing ever smaller dynamic memory cells (DRAM cells) are a well-known goal in the development of new semiconductors, and optimizing the memory

cells with regard to both the "manufacturing cost" and the "cell density" an ongoing effort. Over the last few years, the cell density on a DRAM chip and, at the same time, the performance of the memory elements have increased dramatically due to various improvements. However, when the cell density on a DRAM chip is increased, it is also necessary to decrease the area of the individual cells in order to be able to maintain a reasonable overall chip size.

Due to the continuous decrease in the structural size of the DRAM cells, problems in contacting the memory cells is an ongoing problem. In particular, effective and area-saving contacts to the word lines and bit lines are required to allow further miniaturization of memory cells.

Additionally, it is also highly desirable for optimizing the manufacturing cost, that dynamic memory cells keep the number of manufacturing steps required as small as possible and at the same time keep the technological complexity as small as possible.

Therefore, in the memory cell of the present invention, a DRAM memory is disclosed such that the word line to which the control electrode region of the access transistor of the memory cell is connected, extends within the semiconductor substrate and can be contacted outside the memory cell region so that no additional contact region leading to the outside for connecting the word line is required in the region of the individual memory cell. To accomplish this, a vertical transistor, such as a vertical MOSFET, in connection with a buried word line, is used in the memory cell, and the channel region of the vertical transistor extends inside the trench of the trench capacitor of the memory cell. In addition, the control electrode region, i.e. the gate terminal region, of the vertical transistor is connected to the buried word line region located in the semiconductor substrate.

The control electrode region of the vertical MOSFET can, for example, either be connected only to the buried word line in a predetermined limited region, or as an example only, the control electrode region of the vertical MOSFET can also be formed as a so-called "surrounded gate terminal region" where the gate terminal region completely surrounds the channel region of the MOSFET. Thus, a vertical tunnel MOSFET can be employed in the present invention with exceptional advantage.

It is obvious from the above discussion that Alsmeier, *et al.* does not give a person skilled in the art any motivation to deviate from the teaching presented therein with regard to the arrangement of a DRAM semiconductor cell array. Consequently, the subject matter of the claims cannot be rendered obvious by the disclosure of Alsmeier, *et al.*

Thus, it has been shown that a memory device that includes the feature of the present invention is neither anticipated nor rendered obvious by the prior art, and reconsideration of the rejection is respectfully requested.

Per Examiner's requirement, a marked up copy of the drawings are included herewith as well as formal drawings submitted as replacement sheets showing the Prior Art label on FIGs. 4A, 4B, 5A, and 5B.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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ANNOTATED SHEET
SHOWING CHANGES

FIG 4B
PRIOR ART

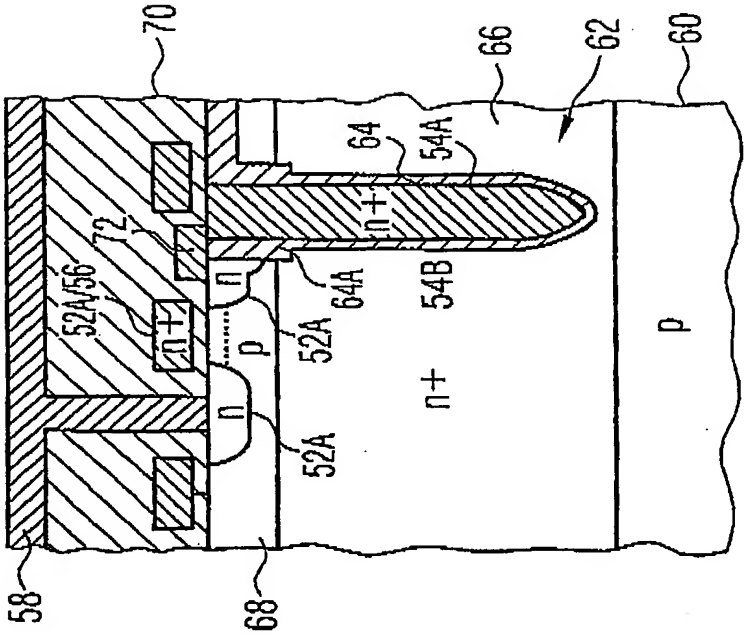

FIG 4A
PRIOR ART

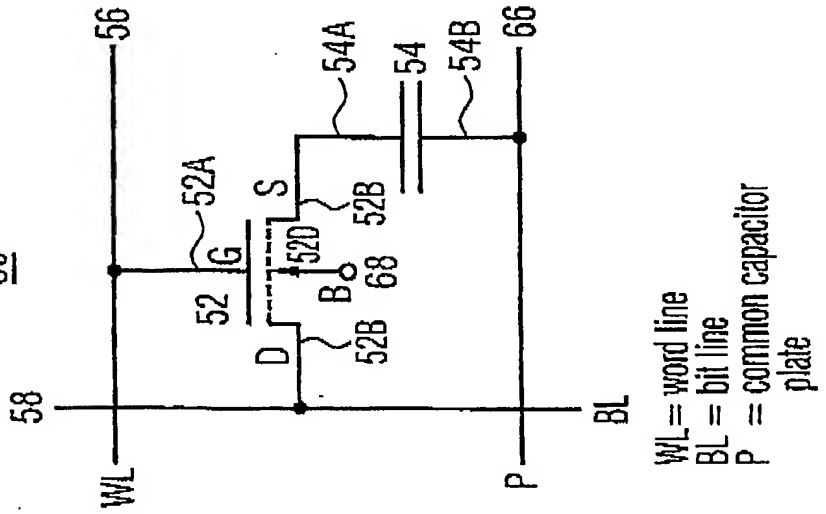

FIG 5A
PRIOR ART

vertical MOSFET

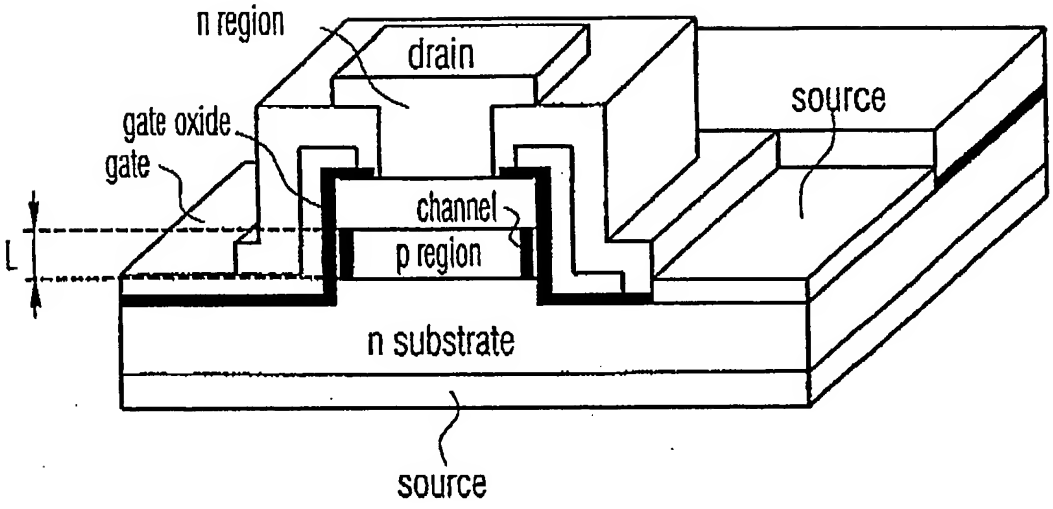

FIG 5B
PRIOR ART